

CLAIM AMENDMENTS

1. (currently amended) A frequency adaptable semiconductor device, comprising:
 - a clock measurement and processing circuitry;
 - a radio frequency circuitry, communicatively coupled to the clock measurement and processing circuitry, that operates using a first clock signal; and
 - a baseband processing circuitry, communicatively coupled to the clock measurement and processing circuitry, that operates using a second clock signal; andwherein the clock measurement and processing circuitry is operable to receive a clock signal;
 - the clock measurement and processing circuitry determines whether the frequency of the received clock signal ~~substantially~~ comprises at least one of a frequency of the first clock signal and a frequency of the second clock signal; and
 - the clock measurement and processing circuitry is operable to transform the frequency of the received clock signal ~~substantially~~ to at least one of the frequency of the first clock signal and the frequency of the second clock signal when the frequency of the received clock signal fails to ~~substantially~~ comprise at least one of the frequency of the first clock signal and the frequency of the second clock signal.
2. (original) The frequency adaptable semiconductor device of claim 1, wherein the clock measurement and processing circuitry further comprises a measurement circuitry and a fractional-N synthesizer;
 - the measurement circuitry is operable to measure the frequency of the received clock signal;
 - the fractional-N synthesizer is operable to perform mathematical processing to transform the received clock signal substantially into at least one of the first clock signal and the second clock signal.
3. (original) The frequency adaptable semiconductor device of claim 2, wherein the fractional-N synthesizer is operable to perform mathematical processing that

comprises at least one of multiplication, division, and skewing of the received clock signal.

4. (original) The frequency adaptable semiconductor device of claim 3, wherein the at least one of the multiplication and the division further comprises employing a selected at least one constant; and

the selected at least one constant being selected from among a plurality of available constants while considering the frequency of the received clock signal and the at least one of the frequency of the first clock signal and the frequency of the second clock signal.

5. (original) The frequency adaptable semiconductor device of claim 1, wherein the clock measurement and processing circuitry further comprises a measurement circuitry;

the measurement circuitry further comprises a comparison circuitry and a microprocessor circuitry; and

the comparison circuitry being communicatively coupled to the microprocessor circuitry.

6. (original) The frequency adaptable semiconductor device of claim 1, wherein the clock measurement and processing circuitry further comprises a fractional-N synthesizer;

the fractional-N synthesizer further comprises a phase locked loop, a divider, a multiplexor, and a gate;

the phase locked loop being communicatively coupled to the divider;

the divider being communicatively coupled to the multiplexor; and

the multiplexor being communicatively coupled to the gate.

7. (original) The frequency adaptable semiconductor device of claim 1, wherein the clock measurement and processing circuitry is operable to receive the clock signal from a known external reference clock signal.

8. (original) The frequency adaptable semiconductor device of claim 7, wherein the frequency of the received clock signal substantially comprises 32.768 kHz.

9. (original) The frequency adaptable semiconductor device of claim 1, further comprising a low power oscillator, communicatively coupled to the clock measurement and processing circuitry; and

wherein the clock measurement and processing circuitry is operable to receive the clock signal from the low power oscillator.

10. (original) The frequency adaptable semiconductor device of claim 1, wherein the baseband processing circuitry initially employs the received clock signal as a main system clock; and

the baseband processing circuitry subsequently switches from the received clock signal to the second clock signal, thereafter using the second clock signal as the main system clock.

11. (original) A semiconductor device, comprising:
a baseband processing circuitry that is operable to characterize a frequency of a received clock signal;
a fractional-N synthesizer that is operable to generate an output clock signal having one frequency selected from among a plurality of frequencies, the selected frequency being within the fractional-N synthesizer selected using a feedback programming value;
wherein the baseband processing circuitry initially employs the received clock signal as a baseband processing circuitry main system clock when determining the feedback programming value;
the baseband processing circuitry feeds back the feedback programming value to the fractional-N synthesizer; and
the baseband processing circuitry subsequently operates using the output clock signal, from the fractional-N synthesizer, as the baseband processing circuitry main system clock.
12. (original) The semiconductor device of claim 11, wherein the baseband processing circuitry further comprises a measurement circuitry;
the measurement circuitry characterizes the frequency of the received clock signal by comparing the received clock signal to a known external reference clock signal.
13. (original) The semiconductor device of claim 12, wherein the frequency of the received clock signal substantially comprises 32.768 kHz.
14. (original) The semiconductor device of claim 12, wherein the baseband processing circuitry further comprises a microprocessor circuitry;
the microprocessor circuitry is reset after the measurement circuitry characterizes the frequency of the received clock signal;
the baseband processing circuitry switches from employing the received clock signal as the baseband processing circuitry main system clock to employing the output

clock signal, provided by the fractional-N synthesizer, as the baseband processing circuitry main system clock during the re-setting of the microprocessor circuitry.

15. (original) The semiconductor device of claim 14, wherein the baseband processing circuitry further comprises a state machine, the microprocessor circuitry and the state machine being communicatively coupled; and

the state machine sets a reboot bit of the microprocessor circuitry thereby initiating the reset of the microprocessor circuitry.

16. (original) The semiconductor device of claim 11, further comprising a radio frequency circuitry, communicatively coupled to the fractional-N synthesizer, that employs the received clock signal as a radio frequency circuitry main system clock.

17. (original) The semiconductor device of claim 16, wherein a frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and

a frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz.

18. (original) The semiconductor device of claim 11, wherein the baseband processing circuitry further comprises a measurement circuitry;

the measurement circuitry further comprises a comparison circuitry and a microprocessor circuitry; and

the comparison circuitry being communicatively coupled to the microprocessor circuitry.

19. (original) The semiconductor device of claim 11, wherein the fractional-N synthesizer further comprises a phase locked loop, a divider, a multiplexor, and a gate;

the phase locked loop being communicatively coupled to the divider;

the divider being communicatively coupled to the multiplexor; and

the multiplexor being communicatively coupled to the gate.

20. (original) The semiconductor device of claim 11, wherein the baseband processing circuitry further comprises a microprocessor circuitry; and the microprocessor circuitry determines whether an operational mode of the semiconductor device comprises a low power oscillator bypass mode.

21. (original) A semiconductor device, comprising:

a baseband processing circuitry;

a fractional-N synthesizer, communicatively coupled to the baseband processing circuitry, that is operable to generate an output clock signal having one frequency selected from among a plurality of frequencies, the selected frequency being within the fractional-N synthesizer selected using a feedback programming value; and

wherein the baseband processing circuitry further comprises a measurement circuitry and a state machine, the measurement circuitry and the state machine being communicatively coupled;

the measurement circuitry further comprises a comparison circuitry and a microprocessor circuitry, the comparison circuitry and the microprocessor circuitry being communicatively coupled, the measurement circuitry is operable to characterize a frequency of a received clock signal;

the fractional-N synthesizer further comprises a phase locked loop, a divider, a multiplexor, and a gate;

the phase locked loop being communicatively coupled to the divider;

the divider being communicatively coupled to the multiplexor;

the multiplexor being communicatively coupled to the gate;

the baseband processing circuitry initially employs the received clock signal as a baseband processing circuitry main system clock when determining the feedback programming value;

at least one of the microprocessor circuitry and the state machine determines the feedback programming value and the baseband processing circuitry feeds back the feedback programming value to at least one of the phase locked loop, the multiplexor, and the gate of the fractional-N synthesizer; and

the baseband processing circuitry subsequently operates using the output clock signal, from the fractional-N synthesizer, as the baseband processing circuitry main system clock.

22. (original) The semiconductor device of claim 21, wherein the state machine generates the feedback programming value, the feedback programming value

comprising a multiplexor select feedback signal that determines which input, selected from at least two inputs provided to the multiplexor, is to be selected as an output of the multiplexor.

23. (original) The semiconductor device of claim 21, wherein the state machine generates the feedback programming value, the feedback programming value comprising a gate control feedback signal.

24. (original) The semiconductor device of claim 21, wherein the microprocessor circuitry generates the feedback programming value, the feedback programming value comprising a phase locked loop control feedback signal.

25. (original) The semiconductor device of claim 21, further comprising a radio frequency circuitry, communicatively coupled to the fractional-N synthesizer, that receives at least one additional output clock signal having one frequency selected from among the plurality of frequencies; and

the radio frequency circuitry employs the at least one additional output clock signal as a radio frequency circuitry main system clock.

26. (original) The semiconductor device of claim 25, wherein a frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and

a frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz.

27. (original) The semiconductor device of claim 21, wherein the microprocessor circuitry is reset after the measurement circuitry characterizes the frequency of the received clock signal;

the baseband processing circuitry switches from employing the received clock signal as the baseband processing circuitry main system clock to employing the output

clock signal, provided by from the fractional-N synthesizer, as the baseband processing circuitry main system clock during the re-setting of the microprocessor circuitry.

2827. (currently amended) The semiconductor device of claim 28, wherein the state machine sets a reboot bit of the microprocessor circuitry thereby initiating the reset of the microprocessor circuitry.

29. (original) The semiconductor device of claim 21, wherein measurement circuitry characterizes the frequency of the received clock signal by comparing the received clock signal to a known external reference clock signal; and the frequency of the known external reference clock signal substantially comprises 32.768 kHz.

30. (original) The semiconductor device of claim 21, wherein the microprocessor circuitry determines whether an operational mode of the semiconductor device comprises a low power oscillator bypass mode.

31. (currently amended) A frequency adaptable method, comprising:
receiving a clock signal;
measuring a frequency of the received clock signal;
determining whether the frequency of the received clock signal ~~substantially~~
comprises a frequency that is suitable for use as a baseband processing circuitry main
system clock by a baseband processing circuitry;
determining whether the frequency of the received clock signal ~~substantially~~
comprises a frequency that is suitable for use as a radio frequency circuitry main system
clock by a radio frequency circuitry;
processing the received clock signal, when the received clock signal is not
suitable for use as the baseband processing circuitry main system clock, to generate a
new clock signal that ~~substantially~~ comprises a frequency that is suitable for use as the
baseband processing circuitry main system clock; and
processing the received clock signal, when the received clock signal is not
suitable for use as the radio frequency circuitry main system clock, to generate at least
one additional new clock signal that ~~substantially~~ comprises a frequency that is suitable
for use as the radio frequency circuitry main system clock.

32. (original) The method of claim 31, further comprising providing the
new clock signal to the baseband processing circuitry.

33. (original) The method of claim 31, further comprising providing the
at least one additional new clock signal to the radio frequency circuitry.

34. (original) The method of claim 31, wherein the received clock signal
is derived from a known external reference clock signal.

35. (original) The method of claim 31, wherein the frequency of the
received clock signal substantially comprises 32.768 kHz.

36. (original) The method of claim 31, wherein the frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and the frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz.

37. (original) The method of claim 31, wherein the radio frequency circuitry and the baseband processing circuitry are contained within a semiconductor device; and

further comprising determining whether an operational mode of the semiconductor device comprises a low power oscillator bypass mode.

38. (original) The method of claim 32, further comprising generating the clock signal using an internal, low power oscillator; and

wherein the semiconductor device comprises the internal, low power oscillator.

39. (original) The method of claim 31, wherein the processing of the received clock signal comprises performing at least one of multiplication, division, and skewing to transform the received clock signal into at least one of the new clock signal and the at least one additional new clock signal.

40. (original) The method of claim 31, further comprising initially providing the received clock signal to the baseband processing circuitry; and subsequently providing the new clock signal to the baseband processing circuitry.

41. (currently amended) A frequency adaptable method, comprising:
determining whether an operational mode of a semiconductor device comprises a low power oscillator bypass mode;

generating a clock signal using a low power oscillator when the operational mode ~~substantially~~ comprises the low power oscillator bypass mode, the semiconductor device comprising the low power oscillator, a baseband processing circuitry, and a radio frequency circuitry;

receiving a clock signal from an external source when the operational mode fails to ~~substantially~~ comprise the low power oscillator bypass mode;

measuring a frequency of at least one of the generated clock signal and the received clock signal;

determining whether the frequency of at least one of the generated clock signal and the received clock signal ~~substantially~~ comprises a frequency that is suitable for use as a baseband processing circuitry main system clock by the baseband processing circuitry;

determining whether the frequency of at least one of the generated clock signal and the received clock signal ~~substantially~~ comprises a frequency that is suitable for use as a radio frequency circuitry main system clock by the radio frequency circuitry;

processing at least one of the generated clock signal and the received clock signal, when at least one of the generated clock signals and the received clock signal is not suitable for use as the baseband processing circuitry main system clock, to generate a new clock signal that ~~substantially~~ comprises a frequency that is suitable for use as the baseband processing circuitry main system clock; and

processing at least one of the generated clock signals and the received clock signal, when at least one of the generated clock signals and the received clock signal is not suitable for use as the radio frequency circuitry main system clock, to generate at least one additional new clock signal that ~~substantially~~ comprises a frequency that is suitable for use as the radio frequency circuitry main system clock.

42. (original) The method of claim 41, wherein the frequency of the received clock signal substantially comprises 32.768 kHz.

43. (original) The method of claim 41, wherein the frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and the frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz.

44. (original) The method of claim 41, wherein the baseband processing circuitry further comprises a microprocessor circuitry; and further comprising initially providing the received clock signal to the baseband processing circuitry; re-booting the microprocessor circuitry; and subsequently providing the new clock signal to the baseband processing circuitry.

45. (original) The method of claim 41, wherein the processing of at least one of the generated clock signal and the received clock signal comprises performing at least one of multiplication, division, and skewing to transform the received clock signal into at least one of the new clock signal and the at least one additional new clock signal.

46. (original) A frequency adaptable method, comprising:
starting up a semiconductor device;
starting up an external oscillator, the external oscillator being communicatively coupled to the semiconductor device;
providing an output signal from the external oscillator to the semiconductor device;
determining an operational mode of the semiconductor device;
determining a frequency of the output signal from the external oscillator when the operational mode of the semiconductor device substantially comprises a low power oscillator bypass mode;
determining whether the frequency of the output signal from the external oscillator substantially comprises a frequency that is suitable for use as a main system clock by at least one circuitry portion within the semiconductor device; and
processing the output signal, from the external oscillator, to generate a new clock signal that substantially comprises a frequency that is suitable for use as the main system clock.

47. (original) The method of claim 46, wherein the at least one circuitry portion within the semiconductor device comprises at least one of a baseband processing circuitry and a radio frequency circuitry.

48. (original) The method of claim 47, wherein the frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and
the frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz.

49. (original) The method of claim 46, wherein the frequency of the output signal from the external reference oscillator substantially comprises 32.768 kHz.

50. (original) The method of claim 46, wherein the processing of the output signal, from the external oscillator, performing at least one of multiplication, division, and skewing to transform the output signal into the new clock signal.

51. (original) A frequency adaptable method employed within a semiconductor device, comprising:

receiving a clock signal from an external crystal oscillator;

during power-up, determining whether at least one circuitry portion within the semiconductor device employs an application that requires determination of a frequency of the received clock signal;

initially employing the clock signal as a main system clock within the semiconductor device;

determining whether a fractional-N synthesizer, contained within the semiconductor device, initially provides the main system clock;

measuring the clock signal that is received from the external crystal oscillator;

allowing a phase locked loop, contained within the fractional-N synthesizer, to lock at a system operating frequency;

resetting a microprocessor circuitry, contained within the semiconductor device;

gating off the clock signal that is received from the external crystal oscillator;

programming the fractional-N synthesizer to generate a new clock signal to be used as the system clock, the system clock having the system operating frequency; and

switching in the new clock signal in place of the gated off clock signal, the new clock signal thereafter being used as the system clock.

52. (original) The method of claim 51, wherein the semiconductor device comprises a radio frequency circuitry and a baseband processing circuitry.

53. (original) The method of claim 52, further comprising operating the radio frequency circuitry by using the clock signal that is received from the external crystal oscillator as the radio frequency circuitry system clock;

initially operating the baseband processing circuitry by using the clock signal that is received from the external crystal oscillator as the baseband processing circuitry system clock; and

subsequently operating the baseband processing circuitry by using the new clock signal that is generated fractional-N synthesizer as the baseband processing circuitry system clock.

54. (original) The method of claim 53, wherein the frequency of the radio frequency circuitry main system clock substantially comprises 192 MHz; and the frequency of the baseband processing circuitry main system clock substantially comprises 48 MHz.

55. (original) The method of claim 51, wherein a frequency of the clock signal from the external oscillator substantially comprises 32.768 kHz.